ABSTRACT OF THE DISCLOSURE

A clock data recovery circuit has a good jitter tolerance characteristic and a broad data recovery range in the event of a wander, that is, a good wander-tracking characteristic of a recovered clock signal. The clock data recovery circuit executes control to compare the position of the edge of data with the position of the edge of a data recovery clock signal (a recovered clock signal) and keeps the clock edge away from the data edge if a gap between the edges becomes smaller than a reference value. A cycle of a reference clock signal is divided into N portions to generate N clock signals (pl) with phases different from each other in composition circuits. By executing control to turn on 2 of the N selector control signals supplied to each 2 adjacent pins of the N-1 selectors at the same time, the N-1 selectors are capable of generating a middle phase between first and second phases and, hence, generating one of N × 2 phases from N input phases as the phase of the data recovery clock signal.